

# Performance estimation of flash analog-to-digital converter using resonant-tunneling MML/MOBILE logic gates

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## Abstract

We have estimated the performance of a flash analog-to-digital converter (ADC) that consists of ternary quantizers and a ternary-to-binary encoder using resonant-tunneling diodes (RTDs). The ternary quantizers consist of resonant-tunneling monostable-to-multistable transition logic (MML) circuits, while the encoder consists of multiple-valued multiple-input monostable-to-bistable transition logic elements ( $M^2$ -MOBILES). By assuming InP-based RTDs and heterojunction field-effect transistors (HFETs), we have carried out SPICE simulation that demonstrates a 4-bit, 10-GS/s ADC operation with a power dissipation of 0.23 W. The input bandwidth, which is defined as a frequency at which the effective number of bit decreases by 3 dB, was estimated to be 500 MHz.

## 1. Introduction

Analog-to-digital converters (ADCs) with sampling frequencies over a few GHz have been required in the field of ultrahigh-speed instrumentation. Recently, they are also expected to play a crucial role in future wireless communications systems. We have proposed an ultrahigh-speed flash ADC using InP-based resonant-tunneling diodes (RTDs), which are known as the fastest semiconductor devices [1, 2]. These ADCs used ternary quantizers consisting of RTD-based monostable-to-multistable transition logic (MML) [3]. We also used an encoder circuit consisting of monostable-bistable transition logic elements [4] that operated in a multiple-valued multiple-input mode ( $M^2$ -MOBILE).

In this paper, we will describe the performance of such an RTD-based flash ADC that uses MML/ $M^2$ -MOBILE gates. We have carried out HSPICE simulation by assuming InP-based RTD and heterojunction field-effect transistor (HFET) technology, and demonstrated a 4-bit, 10-GS/s ADC operation.

The structure of this paper is as follows. First, we explain the circuit configuration and operation principle of an MML ternary quantizer, and an  $M^2$ -MOBILE circuit used in the ternary-to-binary encoder. Then, a 4-bit ADC consisting of MML/ $M^2$ -MOBILE gates is described. Finally, HSPICE simulation results are presented, and static and dynamic characteristics are discussed.

## 2. Circuit Blocks

### 2.1 MML quantizer

The circuit configuration of an MML ternary quantizer is shown in Fig. 1(a). This circuit consists of four RTDs connected in series and two HFETs. The input signal voltage is applied to HFET  $M_1$ . Two threshold voltages,  $V_T^1$  and  $V_T^2$ , are obtained as shown in Fig. 1(b). Three voltage levels, “2,” “1,” and “0,” correspond to the number of switched-off RTDs between the output1 terminal and ground. The voltage level at the output2 terminal is determined by RTD Y. Therefore, as the input voltage  $V_{in}$  increases,  $V_{out1}$  and  $V_{out2}$  change as “2-1-0” and “1-0-0,” respectively, as shown in Fig. 1(c). The MML circuit has the other HFET  $M_2$  with a control voltage  $V_c$ . This is used to vary threshold voltages. The two threshold voltages decrease as  $V_c$  increases, because the linear sum of the drain current of  $M_1$  and  $M_2$  changes the effective peak current of X and Y.

### 2.2 $M^2$ -MOBILE

The circuit configuration of  $M^2$ -MOBILE that was used in the ternary-to-binary encoder is shown in Fig. 2(a). The circuit consists of two RTDs and two HFETs. RTD B switches earlier than RTD A when the input voltage  $V_{in1}$  is large enough. Similarly, RTD A switches earlier when the input voltage  $V_{in2}$  is large enough. We designed device parameters, such as the RTD area and HFET gate width, so that when  $V_{in1} < V_{in2}$ , RTD B switches off and the output voltage  $V_{out}$

is “high,” while RTD A switches off and output voltage  $V_{out}$  is “low” for  $V_{in1} > V_{in2}$ .

The  $M^2$ -MOBILE subtraction operation is explained in Fig. 2(b). Two planes, “ $A+M_1$ ” and “ $B+M_2$ ,” show the sum of the RTD and HFET currents. The intersection corresponds to the border between the high and low outputs because the RTD with the smaller current sum switches earlier and the maximum voltage of  $V_{CLK}$  is chosen so that only one RTD switches off. The output voltage  $V_{out}$  is thus determined as shown in Fig. 2(c), and the binary output corresponds to the subtraction of the two ternary inputs is obtained.

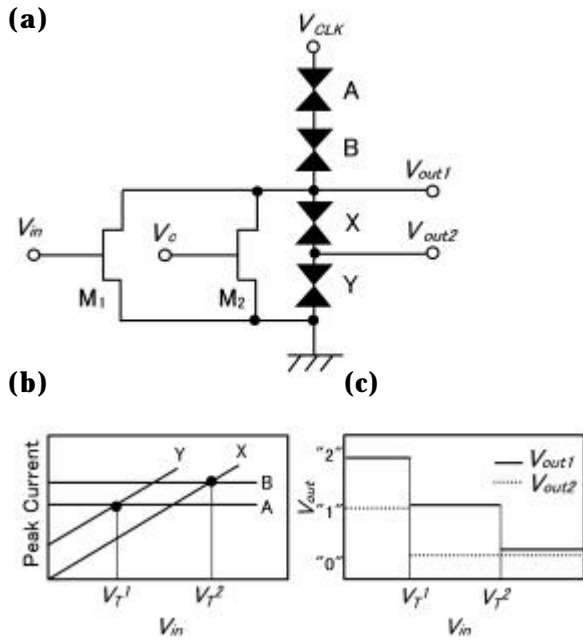


Figure 1. MML quantizer.

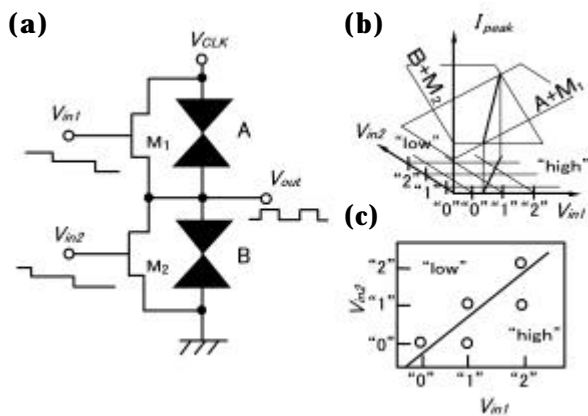


Figure 2.  $M^2$ -MOBILE subtraction circuit.

### 3. 4-bit ADC with MML/ $M^2$ -MOBILE

Now we will explain a 4-bit flash ADC using MML and  $M^2$ -MOBILE gates explained in the previous section. The architecture of a present 4-bit flash ADC is shown in Fig. 3(a).

In accordance with the input voltage  $V_{in}$ , ternary signals are generated from the quantizers represented as MOBILE and MMLs. These signals are then fed to INVERTER for MSB and  $M^2$ -MOBILE subtraction circuits for the other bits, and converted into the binary Gray-code signal output.

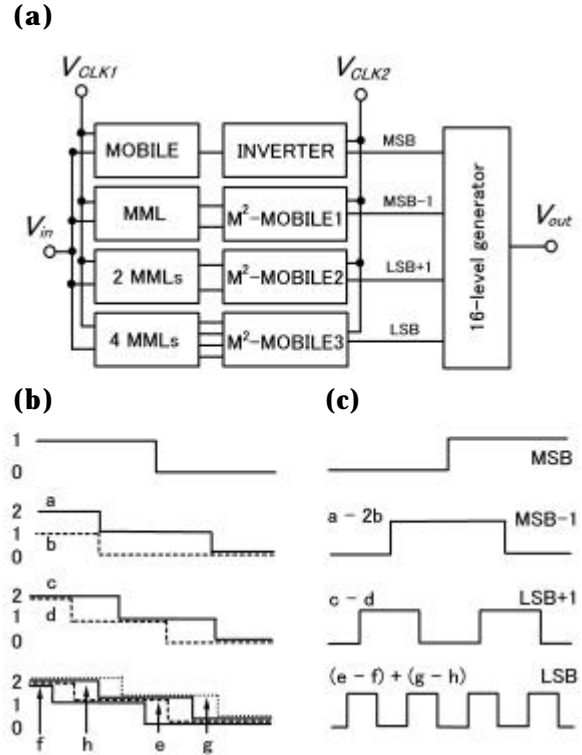


Figure 3. 4-bit ADC architecture.

The quantizer output waveforms are schematically shown in Fig. 3(b), and binary Gray-code outputs from the INVERTER and  $M^2$ -MOBILE subtraction circuits are shown in Fig. 3(c). For MSB, the output signal from the quantizer MOBILE is fed into INVERTER, and the “0-1” signal is obtained. For MSB-1, the “2-1-0” output, “a,” is obtained at the output1 terminal of the MML, while the “1-0-0” output, “b,” is obtained at the output2 terminal of the same MML (see Fig. 1(a)). Then, the following  $M^2$ -MOBILE1 subtraction circuit generates the “0-1-0” signal, “a-b.” It should be noted that “b” is amplified by a factor of two. This is achieved by using HFET  $M_2$  in  $M^2$ -MOBILE with a gate width two times wider than that of HFET  $M_1$  in Fig. 2(a).

For LSB+1, the “2-1-0” output, “c,” is obtained at output1 terminal of one MML, and the “2-1-0” output, “d,” is obtained at the output1 terminal of another MML. Then, the following  $M^2$ -MOBILE2 subtraction circuit generates the “0-1-0-1-0” signal,

“c-d,” as the LSB+1 output. For LSB, the “2-1-0” outputs with different the threshold voltages, “e,” “f,” “g” and “h,” are obtained at the output1 terminal of MMLs. Then, the following M<sup>2</sup>-MOBILE3 subtraction circuit generates the “0-1-0-1-0-1-0-1-0” signal, “(e-f)+(g-h),” as the LSB output. This is achieved by using HFET M<sub>3</sub> and HFET M<sub>4</sub> in M<sup>2</sup>-MOBILE, which are connected with M<sub>1</sub> and M<sub>2</sub> in parallel, respectively.

For the purpose of ADC performance estimation, we used a behavior model of ideal 16-level generator that converts the 4bit Gray code into a 16-level output signal.

## 4. SPICE Simulation Results

### 4.1 Static Characteristics

HSPICE simulation results will be described for the present 4bit, 10-GS/s ADC. We assumed InP-based RTD and 0.1- $\mu$  m HFET technology. The RTD peak current density was  $2 \times 10^5$  A/cm<sup>2</sup> and the peak-to-valley current ratio was 10. The HFET unity-current-gain cutoff frequency  $f_T$  and the maximum oscillation frequency  $f_{MAX}$  were 120 GHz and 200 GHz, respectively.

The ADC operates by two-phase clocked supply voltages,  $V_{CLK1}$  and  $V_{CLK2}$ , as shown in Fig. 3(a). In this simulation, these voltages had the rise time of 50 ps, and the clock period was 100 ps. The clock voltage  $V_{CLK2}$  was delayed by 50 ps compared with  $V_{CLK1}$ .

Figure 4 shows the LSB output waveform of the M<sup>2</sup>-MOBILE3 subtraction circuit when the input signal varies from -0.4 V to 0.4 V with a rise time of 2 ns. This LSB output agrees well with the LSB output characteristic of 4-bit Gray code, i.e., “0-1-0-1-0-1-0-1-0”. Because the clock period is 0.1 ns, this result indicates that the ADC can operate at 10 GS/s.

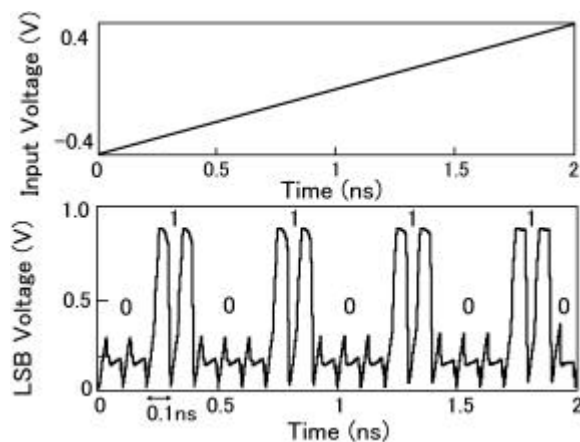


Figure 4. Output waveform.

Figure 5 shows the four output bits of the present ADC as a function of the input signal. Each output value was sampled by an ideal

sample-and-hold circuit included in the 16-level generator behavior model. The input signal rose from -0.4 V to 0.4 V with the rise time of 200 ns. The sampling clock frequency was 10 GHz. The output waveforms certainly show a normal 4-bit ADC operation, and prove that we can obtain 4-bit resolution at 10 GS/s for a quasi-static input signal.

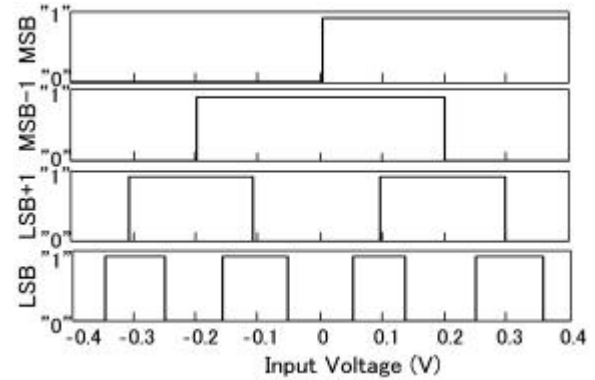


Figure 5. Four outputs of the present ADC.

### 4.2 Dynamic Characteristics

Figure 6 shows the output waveform when the input signal was a 102.5-MHz sinewave with an amplitude of 0.4 V. It is confirmed that the output waveform varied between “0000” and “1111” with 16 digital levels (4-bit) and that there were no missing codes. To calculate the signal-to-noise plus distortion ratio (SNDR), spurious-free dynamic range (SFDR), and effective number of bits (ENOB), we have carried out Fourier analysis. Fig. 7 shows the power spectrum of the output waveform for the input sinewave with a frequency of 102.5 MHz. In this case, SNDR, SFDR, and ENOB were 26.0 dB, 37.6 dB, and 4.0 bit, respectively.

Figure 8 shows the SNDR, SFDR, and ENOB estimated in this manner as functions of the input frequency up to 5 GHz. The sampling frequency was fixed to 10 GHz. Although both the SNDR and SFDR decrease as the input frequency increases, the resolution more than 3.5 bits is obtained up to 500 MHz. The bandwidth, defined as a frequency at which the SNDR decreases by 3 dB, is estimated to be 500 MHz. The device counts in the present ADC are 38 RTDs and 40 HFETs. The power dissipation was also estimated to be 0.23 W at 10-GHz operation.

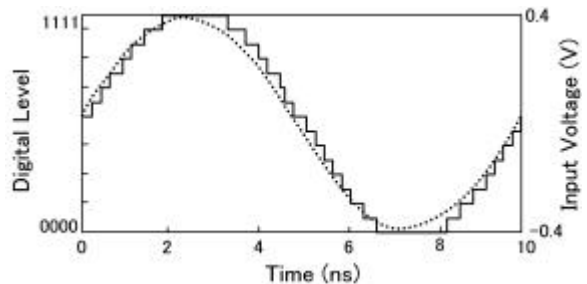
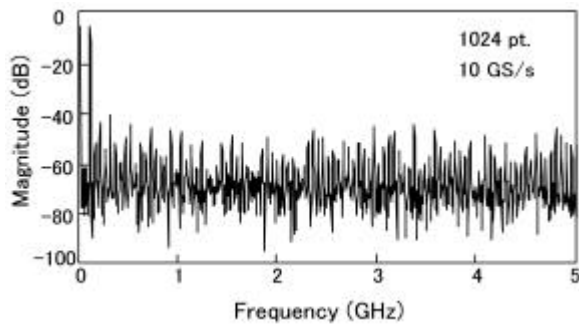
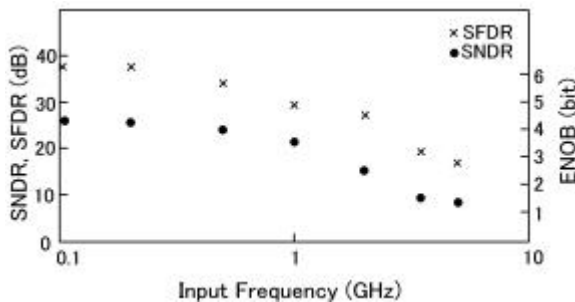


Figure 6. 16-digital-level output waveform.



**Fig 7. Power spectrum.**



**Fig 8. SNDR, SFDR and ENOB.**

## 5. Conclusion

By carrying out HSPICE simulation, we have estimated the RTD-based ADC performance. The compact MML/ $M^2$ -MOBILE gates were used to convert the analog input signal into the binary Gray-code output. For quasi-static input signals, we obtained 4-bit, 10-GS/s flash ADC operation. We also performed Fourier analysis for sinusoidal input signals with frequencies up to 5 GHz. This shows that the input bandwidth was 500 MHz. The Power dissipation at 10 GHz operation was as low as 0.23 W.

## References

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